Amendments to the Specification:

Please replace paragraph **[0001]** with the following amended paragraph:

[0001] This application is a continuation in part of allowed U.S. Patent Application 10/434,977, filed 9 May 2003, which is a continuation in part of pending U.S. Patent Application 10/209,087 filed 30 July 2002. The disclosures of these related applications are incorporated herein by reference.

Please replace paragraph **[0050]** with the following amended paragraph:

[0050] Reference is now made to Figs. 1A and 1B, which schematically illustrate a semiconductor wafer 20 and details of a pattern 22 of contact holes 26 formed thereon, in accordance with an embodiment of the present invention. Fig. 1A is a top view of the wafer, with the pattern shown enlarged in an inset. Fig. 1B is an enlarged, cross-sectional view of the pattern, taken along line 1B-1B in Fig. 1A. Pattern 22 may be a dedicated test pattern, for use in specimen current mapping, as described below, or it may comprise a group of production contact holes in a known location on wafer 20. (Exemplary test patterns are described in the above-mentioned U.S. Patent Application 10/209,087.) Although only the single pattern 22 is shown in Fig. 1A by way of example, multiple patterns of this sort, distributed over the surface of wafer 20, are used in specimen current mapping. The pattern may also include other types of contact openings ~~(not shown)~~, such as trenches or vias. A pattern 22A of trenches 26A is illustrated in Fig. 1C. Alternatively, specimen current measurements may be made and mapped on individual contact holes.